WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first power source node;

a logic gate including, as a component thereof, an insulated gate field effect transistor having a first gate tunnel barrier, for receiving a voltage on a first power source line as an operation power supply voltage and performing a predetermined operation; and

a first switching transistor connected between said first power source node and said first power source line, formed of an insulated gate field effect transistor having a gate tunnel barrier larger than said first gate tunnel barrier, and selectively turned on in response to an operation mode instructing signal instructing an operation mode of said logic gate.

2. The semiconductor device according to claim 1, wherein

said first gate tunnel barrier is equivalent to a gate tunnel barrier of a silicon oxide film having a thickness of 3 nanometers at most.

3. The semiconductor device according to claim 1, wherein

said insulated gate field effect transistor of said logic gate has a gate insulating film of 3 nanometers at most in thickness.

4. A semiconductor device having a standby cycle and an active cycle, and receiving an input signal at a predetermined logical level in said standby cycle, said semiconductor device comprising:

a first insulated gate field effect transistor having a first gate tunnel barrier, connected between a first power source node and a first output node, receiving said input signal on a gate thereof, and made conductive in said standby cycle;

a second insulated gate field effect transistor having a gate tunnel barrier smaller than said first gate tunnel barrier, connected between said first output node and a second power source node, and receiving said input signal on a gate thereof to be made non-conductive in said standby

cycle.

5. The semiconductor device according to claim 4, wherein said first insulated gate field effect transistor has a gate insulating film larger in thickness than a gate insulating film of said second insulated gate field effect transistor.

6. The semiconductor device according to claim 4, further comprising:

a third insulated gate field effect transistor having the second gate tunnel barrier, connected between said first power source node and a second output node, and made non-conductive in said standby cycle according to a signal on said first output node; and

a fourth insulated gate field effect transistor connected between said second output node and said second power source node, made conductive in said standby cycle according to a signal on said first output node, and having the first gate tunnel barrier.

7. A semiconductor device having a standby cycle and an active cycle and receiving an input signal at a predetermined logical level in said standby cycle, comprising:

a first insulated gate field effect transistor connected between a first power source node and a first output node, and receiving said input signal on a gate thereof;

a second insulated gate field effect transistor connected between said first output node and a second power source node, and receiving said input signal on a gate thereof; and

control circuitry coupled to the first and second insulated gate field effect transistors for reducing leak amounts of gate tunnel currents of said first and second insulated gate field effect transistors in said standby cycle below the leak amounts in said active cycle.

8. The semiconductor device according to claim 7, wherein

said control circuitry includes a circuit for making biases of back gates of said first and second insulated gate field effect transistors in said standby cycle deeper than the biases in said active cycle.

9. The semiconductor device according to claim 7, wherein said control circuitry includes a circuit for switching voltage polarities of the first and second power source nodes depending on said standby cycle and said active cycle.

10. The semiconductor device according to claim 7, wherein the first and second insulated gate field effect transistors each have an insulating film providing a gate tunnel barrier substantially not exceeding a gate tunnel barrier provided by a silicon oxide film of 3 nanometers in thickness.

11. The semiconductor device according to claim 7, wherein said control circuitry supplies first and second power source voltages used in a normal operation to the first and second power source nodes in said active cycle, respectively, and supplies third and fourth power supply voltages smaller in absolute value than said first and second power source voltages in said standby cycle, respectively.

12. A semiconductor device having a standby cycle and an active cycle and receiving an input signal of a predetermined logical level in said standby cycle, comprising:

a first insulated gate field effect transistor connected between a first power source node and a first output node, receiving said input signal on a gate thereof, and having a first tunnel barrier; and

a second insulated gate field effect transistor connected between said first output node and a sub-power source node, receiving said input signal on a gate thereof, and rendered conductive complementarily to said first insulated gate field effect transistor, said second insulated gate field effect transistor having a second gate tunnel barrier smaller than said

first gate tunnel barrier; and

a first switching transistor connected between said sub-power supply node and a second power source node, and selectively rendered conductive in response to an operation cycle instructing signal.

13. The semiconductor device according to claim 12, wherein said first switching transistor is made non-conductive in said standby cycle, and has a threshold voltage larger in absolute value than a threshold voltage of said second insulated gate field effect transistor, and said second insulated gate field effect transistor is made non-conductive in response to said input signal in said standby cycle.

14. The semiconductor device according to claim 12, wherein said first insulated gate field effect transistor has a gate insulating film providing a gate tunnel barrier larger than a gate tunnel barrier provided by a silicon oxide film of 3 nanometers in thickness, and said second insulated gate field effect transistor has a gate insulating film providing a gate tunnel barrier substantially not greater than a gate tunnel barrier provided by a silicon oxide film of 3 nanometers in thickness.

15. The semiconductor device according to claim 12, wherein said first switching transistor and said first insulated gate field effect transistor are different in back gate voltage from each other.

16. A semiconductor device comprising:

a first power source node;

a first power source line;

a first switching transistor connected between said first power source node and said first power source line, and selectively made conductive in response to an operation cycle instructing signal;

a first gate circuit receiving a voltage on said first power source line as an operation power supply voltage, said first gate circuit including

an insulated gate field effect transistor as a component thereof;

a second power source node;

a second power source line separately arranged from said first power source line;

a second switching transistor connected between said second power source node and said second power source line, and selectively rendered conductive in phase with said first switching transistor in response to said operation cycle instructing signal; and

a second gate circuit receiving a voltage on said second power source line as an operation power supply voltage thereof, said second gate circuit including an insulated gate field effect transistor as a component thereof,

a ratio between a size of a transistor of said first gate circuit connected to said first power source line and a size of said first switching transistor is substantially equal to a ratio between a size of a transistor of said second gate circuit connected to said second power source line and a size of said second switching transistor, with said size given by a ratio between a channel width and a channel length of an insulated field effect transistor.

17. The semiconductor device according to claim 16, wherein

said first gate circuit includes a first unit gate circuit including a first insulated gate field effect transistor connected to said first power source line, receiving a first input signal on a gate thereof and having a first gate insulating film thickness, and a second insulated gate field effect transistor connected to a third power source line, receiving said first input signal on a gate thereof and having a second gate insulating film thickness greater than said first gate insulating film; and

said second gate circuit includes a second unit gate circuit including a third insulated gate field effect transistor having a source connected to said second power source line, receiving a second input signal on a gate thereof and having said first gate insulating film thickness, and a fourth insulated gate field effect transistor having a

source connected to a fourth power source line, receiving said second input signal on a gate thereof and having said second gate insulating film thickness.

18. The semiconductor device according to claim 16, further comprising:

a replica circuit including a replica switching transistor and a replica gate circuit having a size ratio equal to a ratio between a size of either one of the insulated gate field effect transistor connected to said first power source line of said first gate circuit and the insulated gate field effect transistor connected to said second power supply line of said second gate circuit and a size of either one of the first and second switching transistors, said replica switching transistor supplying an operation power source voltage to said replica gate circuit; and

transmission circuitry for transmitting a voltage corresponding to the operation power source voltage of said replica gate circuit to the first and second power source lines in response to said operation cycle instructing signal.

19. The semiconductor device according to claim 18, wherein

said transmission circuitry includes a comparing circuit for comparing the operation power supply voltage of said replica gate circuit with a voltage on an internal output node, and driving the voltage on said internal output node in accordance with a result of comparison, and

a switching circuit for coupling said internal output node to each of the first and second power source lines in response to said operation cycle instructing signal.

20. The semiconductor device according to claim 16, further comprising:

a switching circuit for coupling the first and second power source lines together in response to said operation cycle instructing signal.

21. The semiconductor device according to claim 16, further comprising:

a third gate circuit connected in cascade with said first gate circuit for receiving an output signal of said first gate circuit, said third gate circuit receiving the voltages on said first power source node and a third power source line as operation power supply voltages thereof, and including an insulated gate field effect transistor as a component thereof;

a fourth gate circuit connected in cascade with said second gate circuit for receiving the voltages on said second power source node and a fourth power source line as operation power supply voltages thereof, and including an insulated gate field effect transistor as a component thereof;

a third switching transistor connected between said third power source line and said third power source node, and rendered conductive and non-conductive in phase with said first switching transistor in response to said operation cycle instructing signal; and

a fourth switching transistor connected between said fourth power source line and said fourth power source node, and rendered conductive and non-conductive in phase with said second switching transistor in response to said operation cycle instructing signal,

a ratio between a size of said third switching transistor and a size of an insulated gate field effect transistor connected to said third power source line in said third gate circuit being equal to a ratio between a size of said fourth switching transistor and a size of an insulated gate field effect transistor connected to said fourth power supply line in said fourth gate circuit.

22. The semiconductor device according to claim 21, wherein

the insulated gate field effect transistor connected to said first power source node in said first gate circuit has a second gate insulating film thickness, and the insulated gate field effect transistor connected to said third power source line in said first gate circuit has a first gate insulating film thickness larger than said second gate insulating film thickness, and

the insulated gate field effect transistor connected to said second power source node in said fourth gate circuit has said second gate insulating film thickness, and the insulated gate field effect transistor connected to said fourth power supply line in said fourth gate circuit has said first gate insulating film thickness.

23. The semiconductor device according to claim 21, further comprising:

a replica circuit including a replica switching transistor and a replica gate circuit having a size ratio equal to a ratio between a size of either one of the insulated gate field effect transistor connected to said third power source line of said third gate circuit and the insulated gate field effect transistor connected to said fourth power source line of said fourth gate circuit and a size of either one of the third and fourth switching transistors, said replica switching transistor supplying an operation power supply voltage to said replica gate circuit; and

transmission circuitry for transmitting a voltage corresponding to the operation power supply voltage of said replica gate circuit to the third and fourth power source lines in response to said operation cycle instructing signal.

24. The semiconductor device according to claim 23, wherein

said transmission circuitry includes a comparing circuit for comparing the operation power supply voltage of said replica gate circuit with a voltage on an internal output node, and driving the voltage on said internal output node in accordance with a result of comparison, and

a switching circuit for coupling said internal output node to each of the first and second power source lines in response to said operation cycle instructing signal.

25. The semiconductor device according to claim 21, further comprising a switching circuit for coupling the third and fourth power source lines in response to said operation cycle instructing signal.

26. A semiconductor device comprising:

a precharge insulated gate field effect transistor for precharging a precharge node to a predetermined voltage in response to activation of a precharge instructing signal, said precharge insulated gate field effect transistor having a first gate tunnel barrier; and

a gate circuit coupled to said precharge node, kept in a standby state during an active state of said precharge instructing signal, and driving said precharge node in accordance with an applied signal in an inactive state of said precharge instructing signal, said gate circuit including, as a component thereof, an insulated gate field effect transistor having a second gate tunnel barrier smaller than said first gate tunnel barrier.

27. The semiconductor device according to claim 26, further comprising:

a precharge assisting transistor for precharging said precharge node to said predetermined voltage level in response to a precharge assisting instructing signal made activate upon transition of said precharge instructing signal from the inactive state to the active state, said precharge assisting transistor comprising an insulated gate field effect transistor having said second gate tunnel barrier.

28. The semiconductor device according to claim 26, wherein

said semiconductor device has an active cycle for operating said gate circuit and a standby cycle for placing said gate circuit in the standby state, and further comprises:

a control circuit for activating said precharge instructing signal in response to a sleep mode instructing signal applied in continuation of said standby cycle for at least a predetermined time, and generating a standby instructing signal activated in the standby cycle in deactivation of said sleep mode instructing signal and deactivated upon activation of said sleep mode instructing signal; and

a standby precharge transistor for precharging said precharge node

to said predetermined voltage upon activation of said standby instructing signal, said standby precharge transistor comprising an insulated gate field effect transistor having said second gate tunnel barrier.

29. A semiconductor device having a standby cycle and an active cycle, comprising:

a precharge transistor being activated for a predetermined time upon transition from the standby cycle to the active cycle, for precharging a precharge node to a predetermined voltage; and

a gate circuit for driving said precharge node in accordance with a signal applied in said active cycle, said gate circuit including, as a component thereof, an insulated gate field effect transistor having a first gate tunnel barrier same as said precharge transistor, and said first gate tunnel barrier being not greater than a gate tunnel barrier provided by a silicon oxide film of 3 nm (nanometer) in thickness.

30. The semiconductor device according to claim 29, further comprising:

a floating preventing insulated gate field effect transistor for holding said precharge node at a voltage level of a polarity different from a polarity of said predetermined voltage in said standby cycle, said floating preventing insulated gate field effect transistor having a gate tunnel barrier larger than the gate tunnel barrier of said precharge transistor.

31. A semiconductor device comprising:

a normal array having a plurality of normal memory cells;

a redundant array having spare memory cells for repairing a defective normal memory cell having a defect in said normal array;

a normal access circuit for accessing a selected normal memory cell in said normal array, said normal access circuit including, as a component thereof, an insulated gate field effect transistor;

a spare access circuit for accessing the spare memory cell in said

redundant array, said spare access circuit including, as a component thereof, an insulated gate field effect transistor; and

a power supply control circuit for setting a gate tunnel current of the insulated gate field effect transistor of an inactive circuit out of said spare access circuit and said normal access circuit to be smaller than the gate tunnel circuit of the transistor in an active circuit out of the spare and normal access circuits.

32. The semiconductor device according to claim 31, wherein

each of said spare and normal access circuits includes a plurality of sub-access circuits to be activated selectively; and

said power supply control circuit sets the unselected sub-access circuit in said spare and normal access circuits to the state causing a gate tunnel current smaller than the gate tunnel current of the transistor in the selected sub-access circuit.

33. The semiconductor device according to claim 31, further comprising:

a determining circuit for determining which is to be activated between the normal and spare access circuits in accordance with an address signal, and activating one of said normal and spare access circuits in accordance with a result of determination, said determining circuit starting the determining operation before activation of an operation mode instructing signal instructing a memory cell selecting operation.

34. The semiconductor device according to claim 31, further comprising:

a determining circuit for determining which is to be activated between the normal and spare access circuits in accordance with an address signal, and activating one of said normal and spare access circuits in accordance with a result of determination, said determining circuit executing the determining operation asynchronously to an

operation mode instructing signal instructing a memory cell selecting operation.